M-5

HIGH-VOLTAGE FET AMPLIFIERS FOR SATELLITE AND PHASED-ARRAY APPLICATIONS*

A. Ezzeddine, H-L. A. Hung, and H. C. Huang

COMSAT Laboratories Clarksburg, MD 20871

ABSTRACT

The high-voltage FET amplifier (HVFA) configuration for power amplifier applications in satellite communications and phased-array systems can offer substantial improvement in DC-to-RF conversion efficiency. A proof-of-concept experiment, design considerations, and the RF results of MIC implementation at C- and X-band are reported. An X-band MMIC HVFA design is also presented.

INTRODUCTION

Increasing use is being made of GaAs power FET amplifiers in satellite communications and phased-array systems because these amplifiers exhibit high linearity, high reliability, and small size (1),(2). However, the relatively low DC bias voltage (8 to 12 V) of the power FET is a drawback in terms of overall system power efficiency. In satellite transponder applications, an electronic power conditioner (EPC) efficiency of only about 85-percent for the power amplifiers is achieved in converting the satellite bus voltage from 24-48 V to about 10 V. Thus, substantial power is lost in the DC-to-DC conversion. In a phased-array system, this low-voltage, high-current characteristic of the FET results in substantial power loss in the DC voltage distribution network.

To resolve this problem, a new high-voltage FET amplifier (HVFA) design offering considerable power savings was developed. This is apparently the first time that an effective approach to this problem has been implemented and reported.

HIGH-VOLTAGE FET AMPLIFIER CONCEPT

The HVFA design consists of several GaAs FETs DC-connected in series, as shown in Figure 1. The total DC voltage for the HVFA can be increased to any desired value, in particular to equal the system bus voltage. The RF output powers of all the FETs are either parallel-fed to different antenna feeds, as in the phased-array configuration, or combined, as in high-power amplifier satellite applications. To provide the necessary RF isolation between the FETs, each source is RF-grounded through a capacitor of appropriate value, while the source of one FET is DC-connected to the drain of another through an inductor.

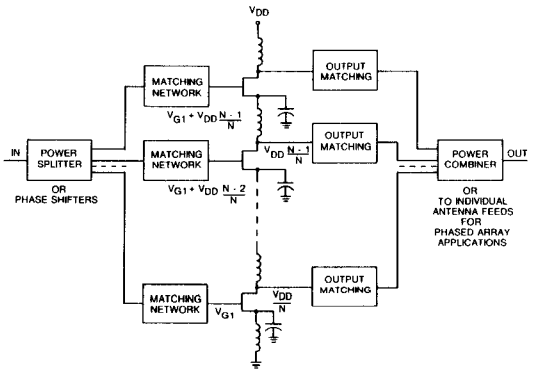

Figure 1. N-Cell HVFA

The new design has several advantages over conventional power FET configurations:

a. In the high-power amplifier design, instead of using large multiple-cell FETs, smaller units can be configured into an HVFA, partially matched individually, and then combined to achieve simplified matching networks with lower circuit losses.

b. For phased-array systems, the HVFA requires lower DC current from the bus source, thus reducing the ohmic losses by a factor of N^2 where N is the number of DC-series-connected FETs in the HVFA.

c. The EPC for FET power amplifiers in satellites can be replaced with a simple voltage regulation scheme, thus improving overall DC-to-RF efficiency.

To further illustrate the advantage of using the HVFA design in the phased-array system, consider a phased array with 1,000 elements, each fed with a solid-state power amplifier that is biased with a DC voltage of 10 V and a current of 1 A. The total DC power delivered to the phased array would equal 10,000 W. If the DC connecting cable has a resistance of 0.001 Ω, the ohmic loss in the cable would be 1,000 W. This is a considerable fraction of the total DC power.

On the other hand, if each circuit is replaced by a high-voltage amplifier consisting of

*This paper is based on work performed at COMSAT Laboratories under the sponsorship of the Communications Satellite Corporation.

0149-645X/85/0000-0336 $01.00 © 1985 IEEE

four units in series, the DC voltage becomes 40 V and the series current 0.25 A. Hence, the total DC power needed for the FETs remains the same, while the total current required drops to 250 A. This reduction of the total DC current by a factor of 4 results in a power reduction by a factor of 16, i.e., 62.5-W power dissipation in the 0.001-Ω cable. The the power consumption would be reduced even further if more amplifier units were DC-connected in series.

In satellite applications, losses in the voltage distribution network and in the EPC decrease when less current is needed to drive the satellite transponder. By connecting several power amplifiers in series, as in the HVFA, less current is drawn from the EPC and consequently a higher DC-to-DC conversion efficiency can be achieved. Furthermore, by using a simple regulation circuit in series with the HVFA, the circuit can be connected directly to the satellite power bus to achieve even higher DC-to-DC conversion efficiency.

PROOF-OF-CONCEPT EXPERIMENT

A proof-of-concept experiment was performed by connecting two individual C-band amplifiers through external couplers. The FET (WE131J) S-parameters at the operating biases were measured. Load-pull techniques were used to determine the loci of optimal load impedances for output power, power-added efficiency, and third- and fifth-order intermodulation products. Devices with similar characteristics were then selected to achieve optimal HVFA operation and power-combined efficiency.

Because the source capacitance, C, is added to the HVFA configuration, the input impedance, Z_{in}, can have a negative real part at low frequency, as

$$Z_{in} = \left(R_g - \frac{g_m}{\omega^2 C C_{gs}}\right) - j\left(\frac{C + C_{gs}}{\omega C C_{gs}}\right)$$

where

R_g = gate resistance

C_{gs} = gate-to-source capacitance

g_m = FET transconductance

ω = frequency in radian/s

Thus potential instability can occur, and careful circuit designs with schemes such as resistive stabilization bias networks are essential to HVFA design. The frequency range of the amplifier instability can be decreased from high frequency to around 1 GHz by using a source capacitance of sufficiently large value. Below this frequency, resistive loads in the DC bias network can adequately stabilize the complete circuit. By placing these stabilizing resistors in the gate bias network, a very minimal amount of DC power will be dissipated. Therefore, the amplifier DC-to-RF power-added efficiency is not affected.

In addition, to achieve phase balance between the RF circuits, both FET carriers were insulated from ground with a very thin Mylar sheet. This arrangement allowed the required good thermal conductivity from the device-to-ground heat sink to be maintained. Any direct ground required from the FET source terminal was made through a small inductor. The matching networks (including parasitic capacitance and inductance) were then designed by using computer-aided optimization, and a parametric study of amplifier performance was made to ensure stable operation. The measured RF performance of the HVFA was found to be the same as that of the individual amplifier, with the expected 3 dB higher output power.

MIC C-BAND HVFA

The HVFA concept was implemented in MIC form at C-band (Figure 2) using the same type of FETs and alumina substrates in a single amplifier housing. Figure 3 shows the RF performance of the individual amplifiers, which was obtained by replacing the Lange coupler with 50-Ω lines, as in the phased-array configuration. The total bias voltage was 24 V. Results are also presented for the combined HVFA for the high-power configuration, in which the 1-dB compression output power is close to 3 dB higher than that of a single amplifier. This demonstrates that optimal combining in the HVFA configuration can be achieved within the limits of the RF loss in the couplers. The power-added efficiency for each configuration is similar at the 1-dB power compression point.

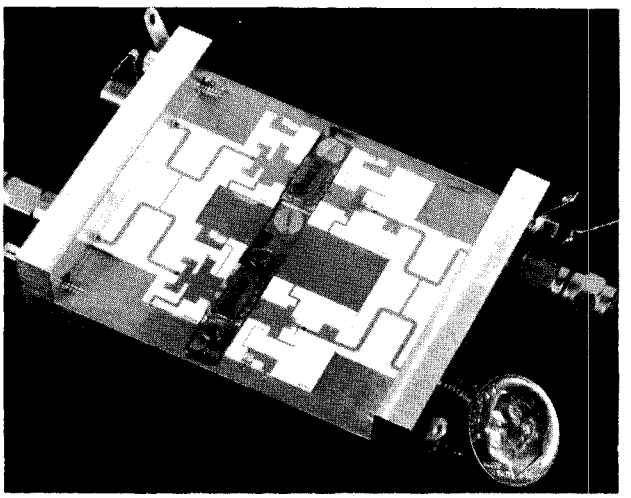

Figure 2. Photograph of C-Band MIC HVFA (High-Power Configuration)

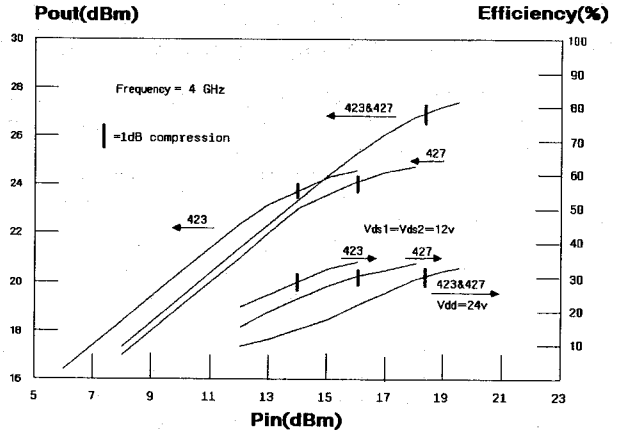

Figure 3. P_{out} and η_{pa} vs P_{in} for C-Band HVFA

The third-order intermodulation distortion of the HVFA was also measured to determine if amplifier linearity would be degraded in the new configuration. Figure 4 shows that comparable results were achieved with the HVFA and the individual amplifiers.

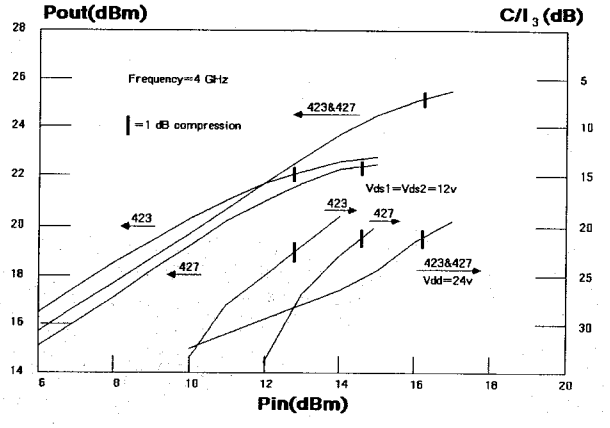

Figure 4. Third-Order IMP vs P_{in} for C-Band HVFA

MIC X-BAND HVFA

Based on extensive characterization of the FLX03WG device, another MIC HVFA operating at X-band was designed (Figure 5) using computer-aided optimization. To minimize circuit loss, matching circuits were fabricated on 15-mil fused-silica substrates. The FLX03WG devices have a measured output power of 26.2 dBm at 11.5 GHz, and a bias voltage of 10 V.

The performance of the HVFA, biased at 20 V in either the combined high-power or phased-array configuration, is illustrated in Figures 6 and 7. The results show no performance degradation with FETs operating in the HVFA configuration. It should be noted that the phase imbalance between the different FETs in the HVFA should be kept to a minimum, especially in high-frequency operations, in order to efficiently combine the output RF power. To minimize the phase imbalance through the method mentioned earlier, both FETs are insulated from the ground plane, although, electrically, one of the FETs has its source terminal at ground potential. Without this arrangement, the optimum efficiency of the HVFA cannot be achieved at X-band or higher frequencies. The HVFA design illustrated can be readily implemented to include more FETs in order to achieve even higher bias voltage.

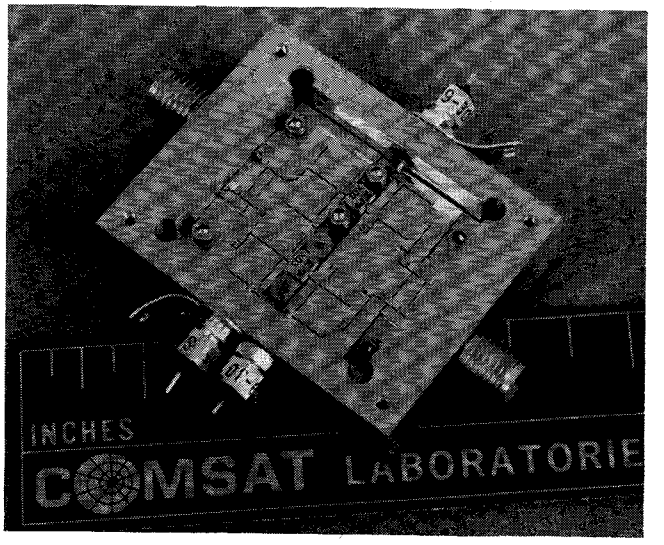

Figure 5. Photograph of X-Band MIC HVFA (High-Power Configuration)

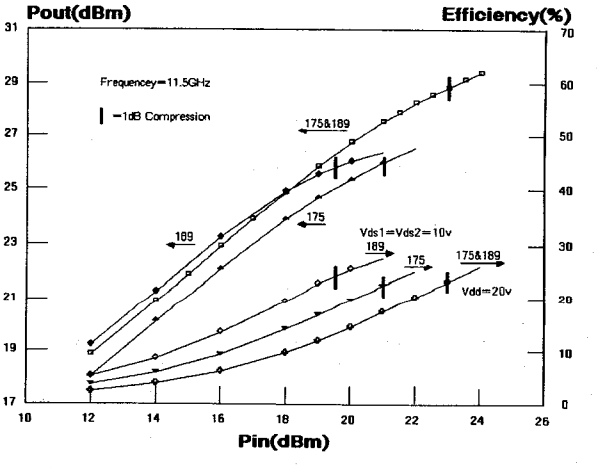

Figure 6. P_{out} and η_{pa} vs P_{in} for X-Band HVFA

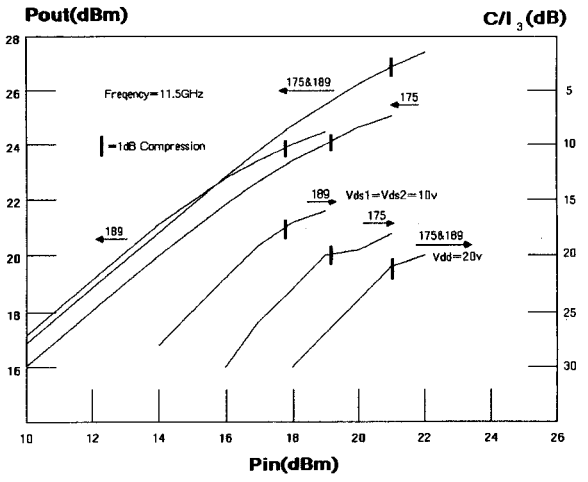

Figure 7. Third-Order IMP vs P_{in} for X-Band HVFA

X-BAND MMIC HVFA DESIGN

The HVFA design concept has been extended to MMICs. Figure 8 shows a completed MMIC design that uses two 0.5 x 750-μm-cell FETs and 10 fabrication process levels. This 2 x 2 mm X-band amplifier has a combined output power comparable to that of the MIC version presented earlier; however, both the FET device and circuit configurations have been optimized for the HVFA operation. Further, with the MMIC approach, degradation in power combined efficiency caused by variation FET characteristics can be minimized. Substantial reduction in the size of the circuit, which is especially advantageous in a phased-array system, can also be achieved.

CONCLUSION

The HVFA is a new circuit configuration suitable for satellite communications and phased-array applications. This circuit offers the same efficiency as conventional FET power amplifiers; however, the higher operating voltage implies lower losses in the DC distribution network, and consequently higher system DC-to-RF power efficiency.

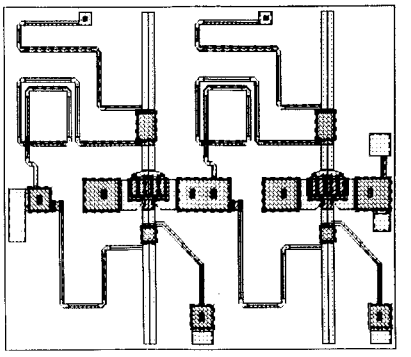

Figure 8. Layout of an X-Band MMIC High-Voltage FET Amplifier

ACKNOWLEDGMENT

The authors would like to thank J. Singer for his support in amplifier assembly and RF measurement.

REFERENCE

(1) B. Dornan et al., "A 4-GHz GaAs FET Power Amplifier: An Advanced Transmitter for Satellite Down-Link Communication Systems," RCA Review, Vol. 41, September 1980, pp. 472-503.

(2) R. J. Mailloux, "Phased Array Theory and Technology," Proc. IEEE, Vol. 70, No. 3, March 1982, pp. 246-288.